

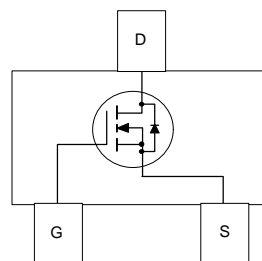
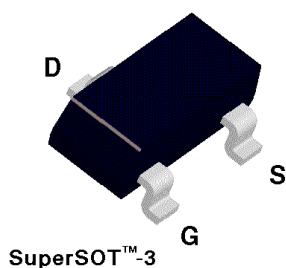
## NDS355N N-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 1.6A, 30V.  $R_{DS(ON)} = 0.125\Omega$  @  $V_{GS} = 4.5V$ .
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.
- Compact industry standard SOT-23 surface mount package.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDS355N	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage - Continuous	20	V
$I_D$	Drain Current - Continuous (Note 1a)	$\pm 1.6$	A
	- Pulsed	$\pm 10$	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
<b>THERMAL CHARACTERISTICS</b>			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to -Case (Note 1)	75	$^\circ\text{C}/\text{W}$

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.6	2	V
			$T_J = 125^\circ\text{C}$	0.5	1.3	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 1.6\text{ A}$			0.125	$\Omega$
			$T_J = 125^\circ\text{C}$		0.25	
			$V_{GS} = 10\text{ V}, I_D = 1.9\text{ A}$		0.085	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	6			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 1.6\text{ A}$		3.5		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		245		pF
$C_{oss}$	Output Capacitance			130		pF
$C_{rss}$	Reverse Transfer Capacitance			20		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		15	30	ns
$t_r$	Turn - On Rise Time			14	30	ns
$t_{D(off)}$	Turn - Off Delay Time			12	25	ns
$t_f$	Turn - Off Fall Time			4	10	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 1.6\text{ A},$ $V_{GS} = 5\text{ V}$		3.5	5	nC
$Q_{gs}$	Gate-Source Charge				1	nC
$Q_{gd}$	Gate-Drain Charge				2	nC

## Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Source Current				0.6	A
I <sub>SM</sub>	Maximum Pulse Source Current (Note 2)				6	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.6 A		0.8	1.2	V

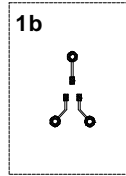
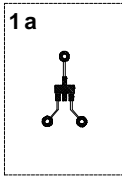
### Notes:

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta J A}(t)} = \frac{T_J - T_A}{R_{\theta J C} + R_{\theta C A}(t)} = I_D^2(t) \times R_{DS(on)} @ T_J$$

Typical R<sub>θJA</sub> using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 250°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2oz copper.
- 270°C/W when mounted on a 0.001 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

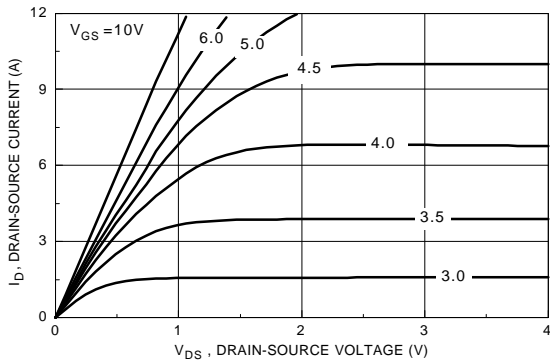


Figure 1. On-Region Characteristics

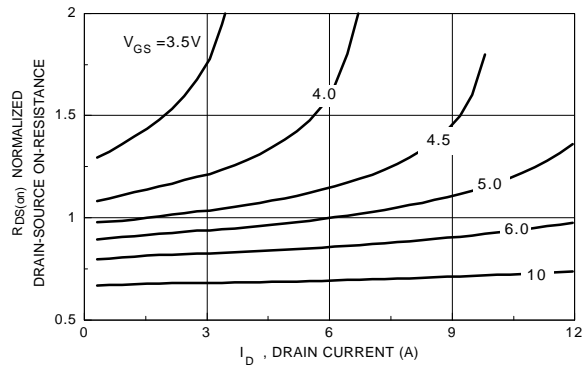


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

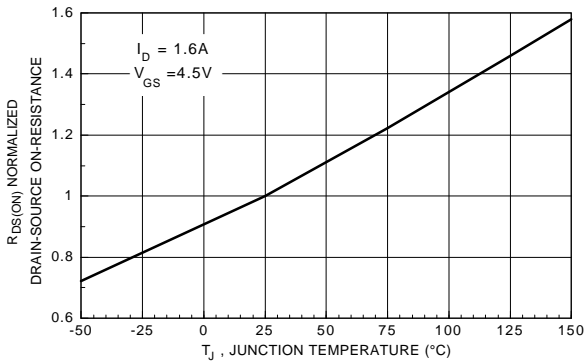


Figure 3. On-Resistance Variation with Temperature

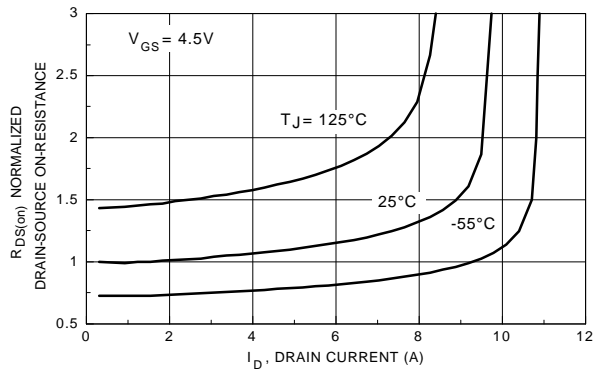


Figure 4. On-Resistance Variation with Drain Current and Temperature

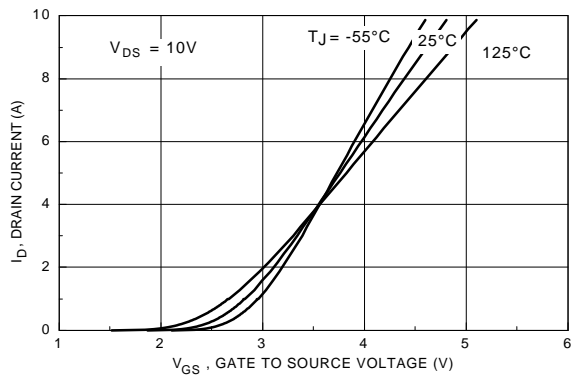


Figure 5. Transfer Characteristics

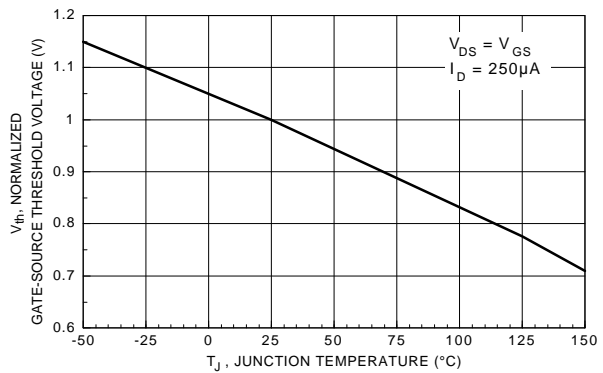
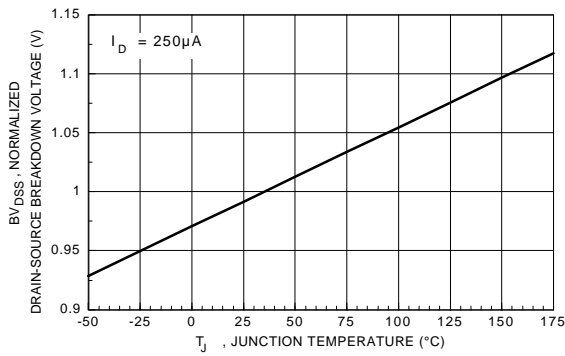
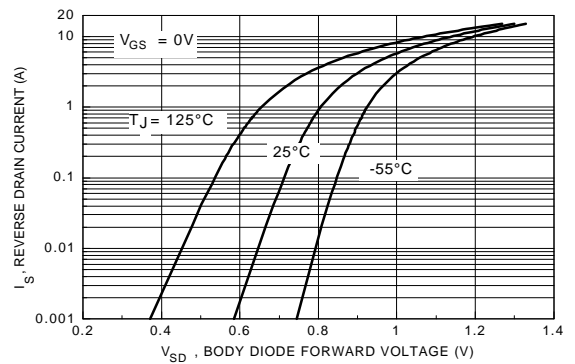


Figure 6. Gate Threshold Variation with Temperature

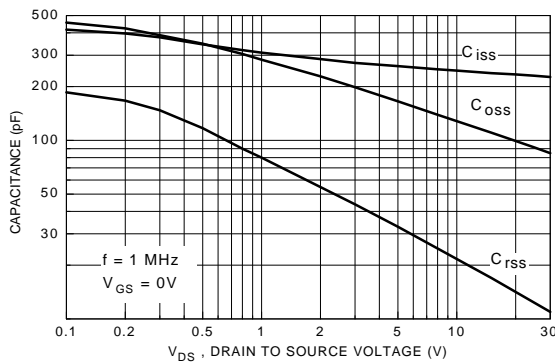
## Typical Electrical Characteristics (continued)



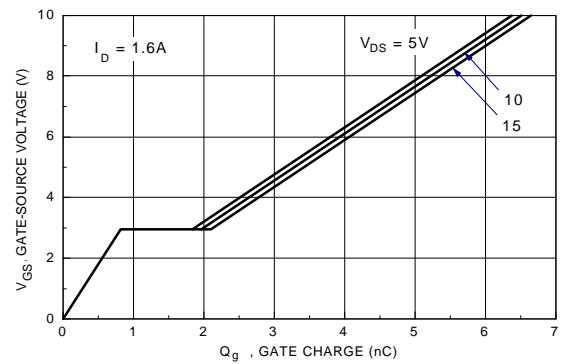
**Figure 7. Breakdown Voltage Variation with Temperature**



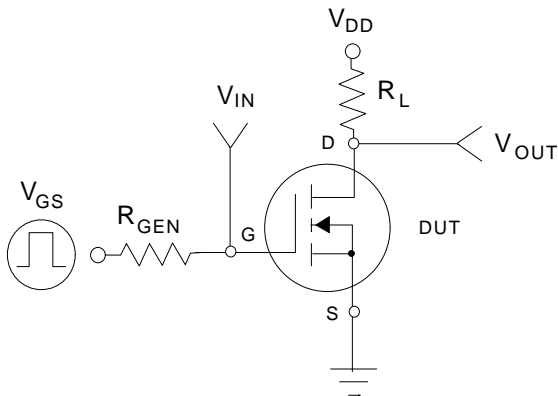
**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature**



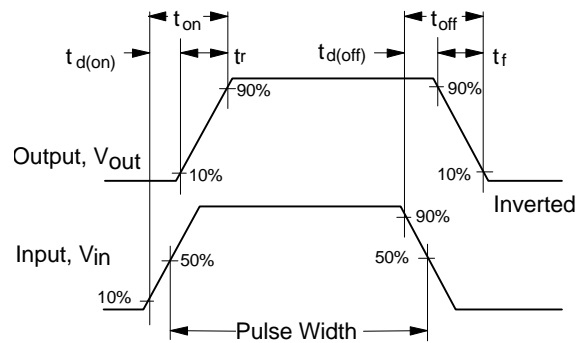
**Figure 9. Capacitance Characteristics**



**Figure 10. Gate Charge Characteristics**

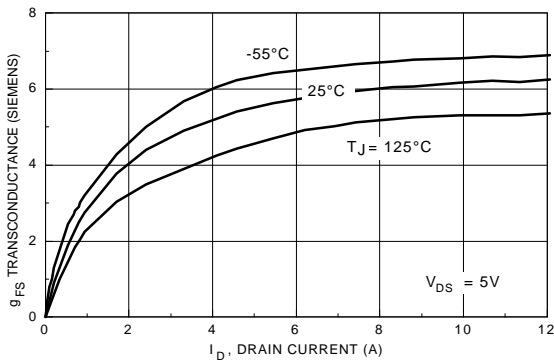


**Figure 11. Switching Test Circuit**

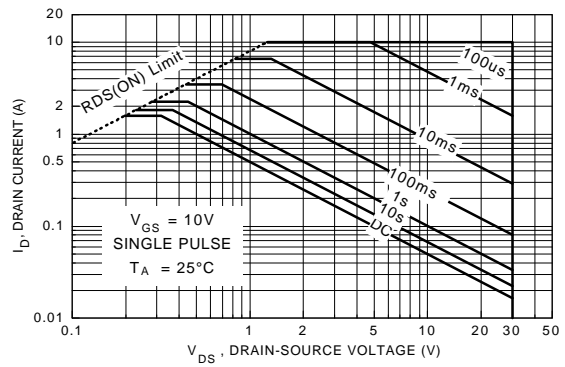


**Figure 12. Switching Waveforms**

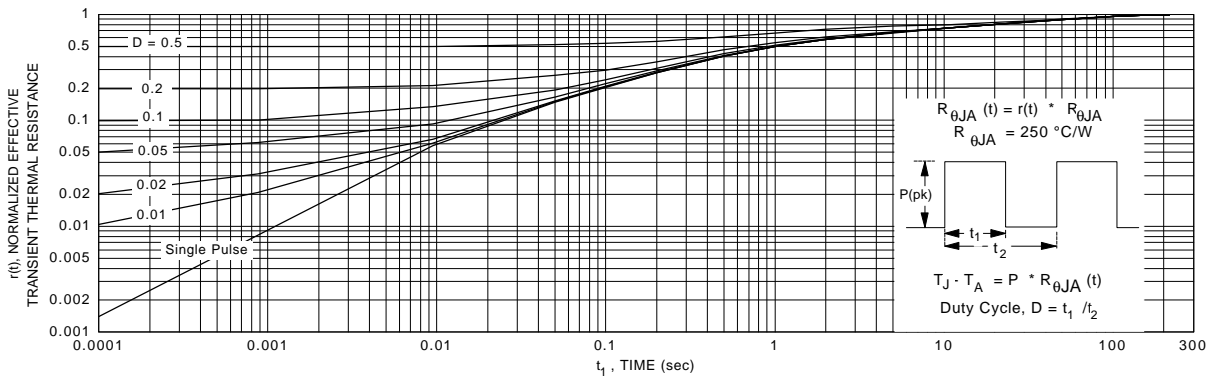
### Typical Electrical Characteristics (continued)



**Figure 13. Transconductance Variation with Drain Current and Temperature**



**Figure 14. Maximum Safe Operating Area**



**Figure 15. Transient Thermal Response Curve**

Note : Characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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